

What i claim d is:

1. A common spacer dual gate memory cell comprising:

5 two bit lines on a semiconductor substrate;
a first channel for a first transistor and a second
channel for a second transistor arranged in series
between said two bit lines;
a first gate dielectric and a second gate dielectric above
10 said first and second channels, respectively;
a first control gate and a second control gate above said
first and second gate dielectrics, respectively; and
a spacer between said first and second control gates;
wherein at least one of said first and second gate
15 dielectrics includes a silicon nitride.

2. A memory cell according to claim 1, further comprising a punch through region between said two bit lines.

20 3. A memory cell according to claim 1, wherein said first control gate extends along a first direction and said second control gate extends along a second direction perpendicular to said first direction.

25 4. A memory cell according to claim 1, wherein said

second control gate has a portion crossing over above and isolated from said first control gate.

5 5. A memory cell according to claim 1, wherein said spacer is formed on a sidewall of said first control gate.

6. A memory cell according to claim 1, wherein said spacer and first control gate extend along a same direction.

10 7. A memory cell according to claim 1, wherein said second control gate has a portion crossing over above said spacer.

15 8. A memory cell according to claim 1, wherein said second control gate has a portion in a trench to contact said second gate dielectric.

9. A memory cell according to claim 1, wherein said first and second gate dielectrics each comprises a silicon nitride.

20 10. A memory cell according to claim 9, wherein one of said two transistors is completely turned on during the other one is read.

25 11. A memory cell according to claim 9, wherein one of said two transistors is completely turned on during the other one

is programmed.

12. A memory cell according to claim 1, wherein one of said first and second gate dielectrics includes an oxide only.

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13. A memory cell according to claim 12, wherein said oxide gated transistor is turned on during the other one is programmed.

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14. A memory cell according to claim 12, wherein said oxide gated transistor is turned on during the other one is read.

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15. A memory cell according to claim 1, wherein silicon nitride gated transistor is programmed with two charge storage locations.

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16. A memory cell according to claim 15, wherein said two charge storage locations are programmed with a threshold voltage substantially different from each other.

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17. A memory cell according to claim 1, wherein silicon nitride gated transistor is programmed with one charge storage location next to said spacer.

18. A method for forming a nonvolatile memory array,

comprising the steps of:

forming a plurality of first gates each with a first gate dielectric on a semiconductor substrate and a plurality of space regions each between two of said plurality of first gates;

implanting a plurality of bit lines each on one side of one of said plurality of first gates;

removing a portion of said first dielectric at said plurality of space regions;

forming a plurality of spacers each on a sidewall of said plurality of first gates;

forming a plurality of second gates with a second gate dielectric at said plurality of space regions; and

forming a plurality of wirings for contacting said plurality of second gate gates;

wherein at least one of said first and second gate dielectrics includes a silicon nitride.

19. A method according to claim 18, wherein said step of forming a plurality of spacers comprises depositing an oxide and etching said oxide for leaving portions thereof on said sidewalls for said plurality of spacers.

20. A method according to claim 18, wherein said first and second gate dielectrics each includes a silicon nitride.

21. A method according to claim 18, wherein one of said first and second gate dielectrics includes an oxide only.

5 22. A method according to claim 18, wherein said step of forming a plurality of first gates comprises the steps of:

 depositing said first gate dielectric on said substrate;

 depositing a polysilicon on said first gate dielectric; and

 patterning said polysilicon and first gate dielectric.

10 23. A method according to claim 22, further comprising forming a cap on said polysilicon.